

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-5 (Cancelled)

1 6. (Currently Amended) A nonvolatile semiconductor
2 memory comprising:

3 (a) a memory cell comprising second semiconductor
4 regions for a source and a drain, respectively, formed in a
5 first semiconductor region in a semiconductor substrate; a
6 charge accumulation layer formed on a region between said
7 second semiconductor regions for the source and the drain,
8 through a gate insulating film; and a control electrode
9 provided on said charge accumulation layer through an
10 insulating film;

11 (b) a third semiconductor region formed between said
12 first semiconductor region and the semiconductor substrate;

13 (c) first voltage application means for applying a
14 voltage to said control electrode;

15 (d) a second voltage application means for applying a
16 voltage to said first semiconductor region; and

17 (e) a third voltage application means for applying a
18 voltage to said third semiconductor region; and
19 (f) means for determining a threshold voltage of said
20 memory cell,
21 wherein a first voltage is applied to said control
22 electrode and a second voltage is applied to said first
23 semiconductor region during a first period, thereby
24 allowing electrons accumulated in said charge accumulation
25 layer to be pulled out into said first semiconductor
26 region,
27 the threshold voltage of said memory cell is
28 determined in a second period following said first period,
29 if it is determined that the threshold voltage of said
30 memory cell is higher than a predetermined threshold
31 voltage, the first voltage is applied to said control
32 electrode and the second voltage is applied to said first
33 semiconductor region in a third period following said
34 second period, thereby allowing the electrons accumulated
35 in said charge accumulation layer to be pulled out into
36 said first semiconductor region, and
37 a third voltage is applied to said third semiconductor
38 region during said first to third periods.

1 7. (Original) A nonvolatile semiconductor memory

2 according to claim 6, wherein

3 a first voltage is applied to the control electrode of
4 said nonvolatile semiconductor memory, and a second voltage
5 is applied to said first semiconductor region; and

6 a potential difference between said first voltage and
7 said second voltage corresponds to a voltage allowing
8 electrons accumulated in said charge accumulation layer to
9 be pulled out into said first semiconductor region.

1 8. (Original) A nonvolatile semiconductor memory

2 according to claim 6, wherein

3 a first voltage is applied to the control electrode of
4 said nonvolatile semiconductor memory, and a second voltage
5 is applied to said first semiconductor region; and

6 a potential difference between said first voltage and
7 said second voltage corresponds to a voltage allowing
8 electrons accumulated in said charge accumulation layer to
9 be pulled out into said first semiconductor region by a
10 tunnel phenomenon.

1 9. (Currently Amended) A nonvolatile semiconductor
2 memory according to claim 6, wherein

3 a first voltage is applied to the control section
4 electrode of said nonvolatile semiconductor memory, a
5 second voltage is applied to said first semiconductor
6 region, and a third voltage is applied to said third
7 semiconductor region; and

8 said third voltage is higher than said second voltage.

1 10. (Original) A nonvolatile semiconductor memory
2 according to claim 6, wherein

3 said nonvolatile semiconductor memory applies a first
4 voltage to said control electrode, and applies a second
5 voltage to said first semiconductor region, thereby pulling
6 out electrons accumulated in said charge accumulation layer
7 into said first semiconductor region, to thereby allow data
8 to be electrically deleted.

1 11. (Original) A nonvolatile semiconductor memory
2 according to claim 6, wherein

3 said nonvolatile semiconductor memory comprises a
4 plurality of memory cell groups each having a plurality of

5 said memory cells formed therein, and the memory cells in
6 each memory cell group are formed above a non-separated
7 third semiconductor region.

1 12. (Original) A nonvolatile semiconductor memory
2 according to claim 6, wherein

3 said nonvolatile semiconductor memory comprises a
4 plurality of memory cell groups each having a plurality of
5 said memory cells formed therein, and the memory cells in
6 each memory cell group are formed above a third
7 semiconductor region separated at intervals of units of a
8 predetermined number of the memory cells.

1 13. (Original) A nonvolatile semiconductor memory
2 according to claim 6, wherein

3 said nonvolatile semiconductor memory comprises a
4 plurality of first memory cell groups each having a
5 plurality of said memory cells in units of a first
6 predetermined number of the memory cells; and a plurality
7 of second memory cell groups each having said memory cells
8 in units of a second predetermined number of the memory
9 cells, the second predetermined number being higher than
10 said first predetermined number;

11 the memory cells in said plurality of first memory
12 cell groups are formed above a third semiconductor region
13 separated at intervals of units of a third predetermined
14 number of the memory cells; and
15 the memory cells in said plurality of second memory
16 cell groups are formed above the third semiconductor region
17 separated at intervals of units of a fourth predetermined
18 number of the memory cells, the fourth predetermined number
19 being higher than the third predetermined number.

Claims 14-17 (Cancelled)

1 18. (Original) A data deletion method for a
2 nonvolatile semiconductor memory, the nonvolatile
3 semiconductor memory comprising:
4 a memory cell comprising second semiconductor regions
5 for a source and a drain, respectively, formed in a first
6 semiconductor region in a semiconductor substrate; a charge
7 accumulation layer formed on a region between said second
8 semiconductor regions for the source and the drain through
9 a gate insulating film; and a control electrode provided on
10 said charge accumulation layer through an insulating film;
11 and

12 a third semiconductor region formed between said first
13 semiconductor region and the semiconductor substrate,
14 wherein
15 the data deletion method comprising the steps of:
16 applying a first voltage to said control electrode,
17 applying a second voltage to said first semiconductor
18 region, and pulling out electrons accumulated in said
19 charge accumulation layer into said first semiconductor
20 region based on a potential difference between said first
21 voltage and said second voltage in a first period;
22 determining a threshold voltage of said memory cell in
23 a second period following said first period; and
24 applying the first voltage to said control electrode,
25 applying the second voltage to said first semiconductor
26 region and thereby pulling out the electrons accumulated in
27 said charge accumulation layer into said first
28 semiconductor region in a third period following said
29 second period if the threshold voltage of said memory cell
30 is higher than a predetermined threshold voltage, and
31 wherein
32 a third voltage is applied to said third semiconductor
33 region during said first to third periods.

1 19. (Original) A data deletion method for a
2 nonvolatile semiconductor memory, according to claim 18,
3 wherein
4 said third voltage is higher than said second voltage.

1 20. (Currently Amended) A nonvolatile semiconductor
2 memory comprising:

3 (a) a memory cell comprising second semiconductor
4 regions for a source and a drain, respectively, formed in a
5 first semiconductor region in a semiconductor substrate; a
6 charge accumulation layer formed on a region between said
7 second semiconductor regions for the source and the drain
8 through a gate insulating film; and a control electrode
9 provided on said charge accumulation layer through an
10 insulating film;

11 (b) a third semiconductor region (NiSO) formed
12 between said first semiconductor region and the
13 semiconductor substrate;

14 (c) first means for applying a voltage to said
15 control electrode;

16 (d) second means for applying a voltage to said first
17 semiconductor region; and

18 (e) third means for prohibiting a voltage from being

19 applied to said third semiconductor region; and

20 (f) means for determining a threshold voltage of said

21 memory cell,

22 wherein the conductive type of said first

23 semiconductor region is a p type and that of said third

24 semiconductor region is an n type,

25 a first voltage is applied to said control electrode

26 and a second voltage is applied to said first semiconductor

27 region in a first period, thereby allowing electrons

28 accumulated in said charge accumulation layer to be pulled

29 out into said first semiconductor region,

30 the threshold voltage of said memory cell is

31 determined in a second period following said first period,

32 if it is determined that the threshold voltage of said

33 memory cell is higher than a predetermined threshold

34 voltage, the first voltage is applied to said control

35 electrode and the second voltage is applied to said first

36 semiconductor region in a third period following said

37 second period, thereby allowing the electrons accumulated

38 in said charge accumulation layer to be pulled out into

39 said first semiconductor region,

40 a second voltage is applied to said first

41 semiconductor region in said first period and thereby said

42 third semiconductor region is charged through said first
43 semiconductor region up to said second voltage, and
44 said third semiconductor region is maintained in a
45 floating state during said first to third periods.

1 21. (Original) A nonvolatile semiconductor memory
2 according to claim 20, wherein
3 a first voltage is applied to the control electrode of
4 said nonvolatile semiconductor memory, and a second voltage
5 is applied to said first semiconductor region; and
6 a potential difference between said first voltage and
7 said second voltage corresponds to a voltage allowing
8 electrons accumulated in said charge accumulation layer to
9 be pulled out into said first semiconductor region.

1 22. (Original) A nonvolatile semiconductor memory
2 according to claim 20, wherein
3 a first voltage is applied to the control electrode of
4 said nonvolatile semiconductor memory, and a second voltage
5 is applied to said first semiconductor region; and
6 a potential difference between said first voltage and
7 said second voltage corresponds to a voltage allowing
8 electrons accumulated in said charge accumulation layer to

9 be pulled out into said first semiconductor region by a
10 tunnel phenomenon.

1 23. (Original) A nonvolatile semiconductor memory
2 according to claim 20, wherein
3 a first voltage is applied to the control electrode of
4 said nonvolatile semiconductor memory by said first means;
5 a second voltage is applied to said first semiconductor
6 region by said second means; and said third semiconductor
7 region is maintained in a floating state by said third
8 means.

1 24. (Original) A nonvolatile semiconductor memory
2 according to claim 20, wherein
3 said nonvolatile semiconductor memory applies a first
4 voltage to said control electrode, and applies a second
5 voltage to said first semiconductor region, thereby pulling
6 out electrons accumulated in said charge accumulation layer
7 into said first semiconductor region, to thereby allow data
8 to be electrically deleted.

1 25. (Original) A nonvolatile semiconductor memory
2 according to claim 20, wherein
3 said nonvolatile semiconductor memory comprises a
4 plurality of memory cell groups each having a plurality of
5 said memory cells formed therein, and the memory cells in
6 each memory cell group are formed above a non-separated
7 third semiconductor region.

1 26. (Original) A nonvolatile semiconductor memory
2 according to claim 20, wherein
3 said nonvolatile semiconductor memory comprises a
4 plurality of memory cell groups each having a plurality of
5 said memory cells formed therein, and the memory cells in
6 each memory cell group are formed above a third
7 semiconductor region separated at intervals of units of a
8 predetermined number of the memory cells.

1 27. (Original) A nonvolatile semiconductor memory
2 according to claim 20, wherein
3 said nonvolatile semiconductor memory comprises a
4 plurality of first memory cell groups each having a
5 plurality of said memory cells in units of a first

6 predetermined number of the memory cells; and a plurality
7 of second memory cell groups each having said memory cells
8 in units of a second predetermined number of the memory
9 cells, the second predetermined number being higher than
10 said first predetermined number;
11 the memory cells in said plurality of first memory
12 cell groups are formed above a third semiconductor region
13 separated at intervals of units of a third predetermined
14 number of the memory cells; and
15 said first semiconductor region having the memory
16 cells in said plurality of second memory cell groups formed
17 therein is formed in the third semiconductor region
18 separated at intervals of units of a fourth predetermined
19 number of the memory cells, the fourth predetermined number
20 being higher than the third predetermined number.

Claims 28-30 (Cancelled)

1 31. (Currently Amended) A data deletion method for a
2 nonvolatile semiconductor memory, the nonvolatile
3 semiconductor memory comprising:
4 a memory cell comprising second semiconductor regions
5 for a source and a drain, respectively, formed in a first

6 semiconductor region in a semiconductor substrate; a charge
7 accumulation layer formed on a region between said second
8 semiconductor regions for the source and the drain through
9 a gate insulating film; and a control electrode provided on
10 said charge accumulation layer through an insulating film;
11 and

12 a third semiconductor region formed between said first
13 semiconductor region and the semiconductor substrate,
14 wherein

15 the data deletion method comprises the steps of:

16 applying a first voltage to said control electrode,
17 applying a second voltage to said first semiconductor
18 region, and pulling out electrons accumulated in said
19 charge accumulation layer into said first semiconductor
20 region based on a potential difference between said first
21 voltage and said second voltage in a first period;

22 determining a threshold voltage of said memory cell in
23 a second period following said first period; and

24 applying the first voltage to said control electrode,
25 applying the second voltage to said first semiconductor
26 region and thereby pulling out the electrons accumulated in
27 said charge accumulation layer, into said first
28 semiconductor region in a third period following said

29 second period if the threshold voltage of said memory cell
30 is higher than a predetermined threshold voltage, and
31 wherein
32 the conductive type of said first semiconductor region
33 is a p type and that of said third semiconductor region is
34 an n type,
35 a second voltage is applied to said first
36 semiconductor region in said first period and thereby said
37 third semiconductor region is charged through said first
38 semiconductor region up to said second voltage, and
39 said third semiconductor region is maintained in a
40 floating state during said first to third periods.

1 32. (Original) A nonvolatile semiconductor memory
2 comprising:
3 (a) a plurality of memory cell groups each having a
4 plurality of memory cells formed on a main surface of a
5 first semiconductor region in a semiconductor substrate,
6 each memory cell comprising second semiconductor regions
7 for a source and a drain, respectively, formed in said
8 first semiconductor region; a charge accumulation layer
9 formed on a region between the second semiconductor regions
10 for the source and the drain through a gate insulating

11 film; and a control electrode provided on said charge
12 accumulation layer through an insulating film;
13 (b) a third semiconductor region formed between said
14 first semiconductor region and the semiconductor substrate;
15 (c) first voltage application means for applying a
16 voltage to said control electrode; and
17 (d) second voltage application means for applying a
18 voltage to said first semiconductor region and said third
19 semiconductor region, respectively, wherein
20 said third semiconductor region is separated at
21 intervals of units of a predetermined number of the memory
22 cells in the plurality of memory cell groups.

1 33. (Original) A nonvolatile semiconductor memory
2 according to claim 32, wherein
3 a first voltage is applied to the control electrode of
4 said nonvolatile semiconductor memory, and a second voltage
5 is applied to said first semiconductor region and said
6 third semiconductor region, respectively; and
7 a potential difference between said first voltage and
8 said second voltage corresponds to a voltage allowing
9 electrons accumulated in said charge accumulation layer to
10 be pulled out into said first semiconductor region.

1 34. (Original) A nonvolatile semiconductor memory
2 according to claim 32, wherein

3 a first voltage is applied to the control electrode of
4 said nonvolatile semiconductor memory, and a second voltage
5 is applied to said first semiconductor region and said
6 third semiconductor region, respectively; and

7 a potential difference between said first voltage and
8 said second voltage corresponds to a voltage allowing
9 electrons accumulated in said charge accumulation layer to
10 be pulled out into said first semiconductor region by a
11 tunnel phenomenon.

1 35. (Original) A nonvolatile semiconductor memory
2 according to claim 32, wherein

3 said plurality of memory cell groups comprise a
4 plurality of first memory cell groups each having a
5 plurality of said memory cells in units of a first
6 predetermined number of the memory cells; and a plurality
7 of second memory cell groups each having said memory cells
8 in units of a second predetermined number of the memory
9 cells, the second predetermined number being higher than
10 said first predetermined number;

11 the memory cells in said plurality of first memory
12 cell groups are formed above a third semiconductor region
13 separated at intervals of units of a third predetermined
14 number of the memory cells; and
15 the memory cells in said plurality of second memory
16 cell groups are formed above the third semiconductor region
17 separated at intervals of units of a fourth predetermined
18 number of the memory cells, the fourth predetermined number
19 being higher than the third predetermined number.

Claims 36-38 (Cancelled)